CLAIMS

1. An apparatus comprising:

at least one processor;

a memory coupled to the at least one processor;

an integrated circuit design residing in the memory, the integrated circuit design including a plurality of logic blocks;

a static timing tool residing in the memory and executed by the at least one processor, the static timing tool performing analysis that results in a plurality of slack computations;

a timing analysis mechanism residing in the memory and executed by the at least one processor, the timing analysis mechanism including a dummy edge mechanism that creates a dummy clock test edge for a selected logic block that has a clock test signal and a data launch signal that are on opposite edges in a manner that results in the dummy clock test edge and the data launch signal being on the same edge, the static timing tool automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block.

2. The apparatus of claim 1 wherein the static timing tool is EinsTimer.

3. The apparatus of claim 1 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

4. The apparatus of claim 1 wherein the timing analysis mechanism improves at least one of the plurality of slack computations using at least one user delta adjust parameter to adjust the clock test signal.

5. The apparatus of claim 1 wherein the timing analysis mechanism provides input to the static timing tool but is not part of the static timing tool.

6. An apparatus comprising:

at least one processor;

a memory coupled to the at least one processor;

an integrated circuit design residing in the memory, the integrated circuit design including a plurality of logic blocks;

a static timing tool residing in the memory and executed by the at least one processor, the static timing tool performing analysis that results in a plurality of slack computations; and

a timing analysis mechanism residing in the memory and executed by the at least one processor, the timing analysis mechanism being separate from the static timing tool and providing input to the static timing tool, wherein the timing analysis mechanism creates a dummy clock test edge for a selected logic block that has a clock test signal and a data launch signal that are on opposite edges in a manner that results in the dummy clock test edge and the data launch signal being on the same edge, the static timing tool automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block using at least one user delta adjust parameter to adjust the clock test signal.

7. The apparatus of claim 6 wherein the static timing tool is EinsTimer.

8. The apparatus of claim 6 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

9. A computer-implemented method for performing static timing analysis on an integrated circuit design, the method comprising the steps of:

identifying a first logic block in the integrated circuit design that includes a clock test signal and a data launch signal that occur on opposite edges;

calculating slack between the clock test signal and the data launch signal;

creating a dummy clock test signal on the first logic block in a manner that the dummy clock test signal and the data launch signal occur on the same edge;

automatically identifying at least one common block through which both the clock test signal and the data launch signal pass before reaching the first logic block; and

adjusting the slack according to delay characteristics through the at least one common block.

10. The method of claim 9 wherein the step of adjusting the slack comprises the steps of:

(A) determining a difference between fastest and slowest delay through the at least one common block;

(B) multiplying the difference in (A) by a correction factor; and

(C) adjusting the slack by the result of the calculation in (B).

11. A computer-implemented method for performing static timing analysis on an integrated circuit design, the method comprising the steps of:

identifying a first logic block in the integrated circuit design that includes a first clock test signal and data launched by a first data launch signal, where the first clock test signal and the first data launch signal occur on the same edge;

calculating a first slack number corresponding to slack between the first clock test signal and the data launched by the first data launch signal;

identifying a second logic block in the integrated circuit design that includes a second clock test signal and data launched by a second data launch signal where the second clock test signal and the second data launch signal occur on opposite edges;

calculating a second slack number corresponding to slack between the second clock test signal and the data launched by the second data launch signal;

creating a dummy clock test edge at the second logic block so the dummy clock test edge and the second data launch signal occur on the same edge;

automatically identifying a first set of common blocks through which both the first clock test signal and the first data launch signal pass before reaching the first logic block;

automatically adjusting the first slack number according to delay characteristics through the first set of common blocks;

automatically identifying a second set of common blocks through which both the second clock test signal and the second data launch signal pass before reaching the second logic block; and

automatically adjusting the second slack number according to delay characteristics through the second set of common blocks.

12. The method of claim 11 wherein the step of automatically adjusting the first slack number comprises the steps of:

(A) determining a difference between fastest and slowest delay through the first set of common blocks; and

(B) adjusting the first slack number by the difference calculated in (A).

13. The method of claim 11 wherein the step of automatically adjusting the second slack number comprises the steps of:

(A) determining a difference between fastest and slowest delay through the second set of common blocks;

(B) multiplying the difference in (A) by a correction factor; and

(C) adjusting the second slack number by the result of the calculation in (B).

14. The method of claim 11 wherein the step of automatically adjusting the second slack number comprises the step of defining at least one user delta adjust parameter for the second clock test signal.

15. A program product comprising:

a timing analysis mechanism that includes a dummy edge mechanism that creates a dummy clock test edge for a selected logic block in an integrated circuit design, the selected logic block having a clock test signal and a data launch signal that are on opposite edges, the dummy edge mechanism creating the dummy clock test edge so the dummy clock test edge and the data launch signal are on the same edge, the timing analysis mechanism automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block; and

computer readable signal bearing media bearing the timing analysis mechanism.

16. The program product of claim 15 wherein the signal bearing media comprises recordable media.

17. The program product of claim 15 wherein the signal bearing media comprises transmission media.

18. The program product of claim 15 wherein the static timing tool is EinsTimer.

19. The program product of claim 15 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

20. The program product of claim 15 wherein the timing analysis mechanism improves at least one of the plurality of slack computations using at least one user delta adjust parameter to adjust the clock test signal.

21. A program product comprising:

a timing analysis mechanism that is separate from a static timing tool and that provides input to the static timing tool, the timing analysis mechanism creating a dummy clock test edge for a selected logic block that has a clock test signal and a data launch signal that are on opposite edges in a manner that results in the dummy clock test edge and a data launch signal on a logic block in an integrated circuit design occurring on the same edge, the timing analysis mechanism automatically identifying in the integrated circuit design at least one common logic block through which the clock test signal and the data launch signal both pass before arriving at the selected logic block, the timing analysis mechanism automatically improving at least one of the plurality of slack computations due to the at least one common logic block using at least one user delta adjust parameter to adjust the clock test signal; and

computer readable signal bearing media bearing the timing analysis mechanism.

22. The program product of claim 21 wherein the signal bearing media comprises recordable media.

23. The program product of claim 21 wherein the signal bearing media comprises transmission media.

24. The program product of claim 21 wherein the static timing tool is EinsTimer.

25. The program product of claim 21 wherein the timing analysis mechanism determines a difference between fastest and slowest delay through the at least one common logic block, multiplies the difference by a correction factor, and adjusts the slack by the difference multiplied by the correction factor.

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